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EXHIBIT G

716 F.2d 1542
219 U.S.P.Q. 189
(Cite as: 716 F.2d 1542)

United States Court of Appeals,
Federal Circuit.

In re Cornelius MULDER and Henricus Elisabeth Jozef Wulms.

Appeal No. 83-647.

Aug. 23, 1983.

Appeal was taken from the United States Patent and Trademark Office Board of Appeals, which affirmed examiner's rejection of certain claims of patent application. The Court of Appeals, Rich, Circuit Judge, held that certain claims of patent application on integrated circuit would be rejected for obviousness in view of prior art disclosed in article, combined with three patents and another article.

Affirmed.

West Headnotes

[1] Patents ⇐90(5)
291k90(5) Most Cited Cases

Applicants were entitled, as of date of constructive reduction to practice, to Netherlands filing date of patent application, where patent was filed in the United States within one year. 35 U.S.C.A. § 119.

[2] Patents ⇐90(5)
291k90(5) Most Cited Cases

Statute providing that when a United States application has been filed within a year from application in a convention country, the formalities all being complied with, the United States application shall have same effect as same application would have if filed in this country on date on which application for patent with the same invention was first filed in such foreign country is a "patent saving" provision for benefit of applicants, and an applicant is entitled to rely on it as a constructive reduction to practice to overcome date of a reference under rule. 35 U.S.C.A. § 119; Patent and Trademark Office Practice Rule 131, 35 U.S.C.A.App.

[3] Patents ⇐16.5(1)
291k16.5(1) Most Cited Cases
(Formerly 291k16.5)

Conception date of July 15, 1974, and constructive reduction to practice date of October 9, 1974, were not coupled with due diligence as required by patent rule governing affidavit or declaration of prior invention to overcome cited patent for publication, and thus publication had to be treated as prior art. Patent and Trademark Office Practice Rule 131, 35 U.S.C.A.App.

[4] Patents ⇐16.5(1)
291k16.5(1) Most Cited Cases
(Formerly 291k16.5)

Certain claims of patent application on integrated circuit were rejected for obviousness in view of prior art disclosed in publication, combined with three patents and another publication.

Patents ⇐328(2)
291k328(2) Most Cited Cases

3,643,235, 4,056,810, 4,076,555. Cited as prior art.
*1542 Steven R. Biren, Tarrytown, N.Y., argued for appellant.

Thomas E. Lynch, Washington, D.C., argued for appellee. With him on the brief were Joseph F. Nakamura, Sol., and Jere W. Sears, Deputy Sol., Washington, D.C.

Before MARKEY, Chief Judge, and RICH and BENNETT, Circuit Judges.

RICH, Circuit Judge.

This appeal is from the July 27, 1982, decision, adhered to on reconsideration October 19, 1982, of the U.S. Patent and Trademark Office (PTO) Board of Appeals (board) affirming the examiner's rejection under 35 U.S.C. § 103 of certain claims [FN1] of *1543 appellants' application, serial No. 602,473, filed August 6, 1975, for "Integrated Circuit." Appellants claim the benefit under 35 U.S.C. § 119 of a convention filing date in the Netherlands of October 9, 1974. We affirm.

FN1. The claims on appeal to the board were 2-5, 7-9, 16-18, 20, 21, 23, 24, 31-33, 35, 39-42, and 44. Claims 29, 30, and 45-47 had been allowed by the examiner. The board reversed the rejection of claims 5, 7, 8, 16-18, 20, 21, 23, 24, and 25. The claims on appeal to this court are 2-4, 9, 31-33, 39-42, and 44.

Our jurisdiction of the appeal is under 28 U.S.C. § 1295(a)(4)(A), (Pub.L. 97-164, Title 1, § 127(a), Apr. 2, 1982, 96 Stat. 37).

Background

This ex parte appeal from the PTO involves appellants' patent application on an integrated circuit, the appealed claims of which stand rejected for obviousness under § 103 in view of prior art disclosed in an article by Rodgers et al., published in the IEEE Journal of Solid State Circuits, Vol. SC- 9, No. 5, pages 247 and 248 (Rodgers), combined with one or more of the following:

Berger et al. U.S. Pat. 3,643,235 Feb. 15, 1972

Hart et al. U.S. Pat. 4,056,810 Nov. 1, 1977
(Parent filed May 15, 1972)

Agraz-Guerena et al. U.S. Pat. 4,076,555 Feb. 28, 1978
(Parent filed Sept. 3, 1974)

de, Troye, Digest of Technical Papers, 1974 IEEE International Solid State Circuits Conference, Feb. 13, 1974, pages 12, 13, and 214.

The real party in interest here is the assignee of appellants, U.S. Philips Corporation, which is affiliated with N.V. Philips Gloeilampenfabrieken of the Netherlands, where the applicants are located. The U.S. patent application was prepared in the Netherlands and sent to the patent department of U.S. Philips Corporation in Briarcliff Manor, N.Y., where it was received on July 15, 1974. A corresponding Netherlands patent application was filed on October 9, 1974. The U.S. application was filed within a year under the International Convention on August 6, 1975, claiming the benefit of the Netherlands filing date under 35 U.S.C. § 119 . The PTO has accorded applicants that date. There is no question that applicants complied with all of the formalities required by § 119 and related PTO rules.

Confronted with rejections of claims based in part, if not primarily, on Rodgers, appellants attempted to antedate, and thus remove, that reference as prior art, by filing declarations under 37 CFR 1.131 (Rule

131). In pertinent part, the rule reads (emphasis ours):

> § 1.131 Affidavit or declaration of prior invention to overcome cited patent or publication.
> (a) When any claim of an application is rejected on reference to a * * * printed publication, and the applicant shall make oath or declaration as to *facts showing a completion of the invention in this country* * * * before the date of the printed publication, then the * * * publication cited shall not bar the grant of a patent to the applicant, unless the date of such * * * printed publication be more than one year prior to the date on which the application was *filed in this country.*
> (b) The showing of facts shall be such, in character and weight, as to establish reduction to practice prior to the effective date of the reference, or *conception of the invention prior to the effective date of the reference coupled with due diligence from said date to a subsequent reduction to practice or to the filing of the application.* Original exhibits of drawings or records, or photocopies thereof, must accompany and form part of the affidavit or declaration or their absence satisfactorily explained.

Applicants proved to the satisfaction of the PTO the receipt in this country of the draft patent application which was accepted as a fact showing conception of the invention prior to Rodgers' publication date, which date is taken by the PTO to be the receipt of the IEEE Journal containing the Rodgers article by the PTO on October 7, 1974. Appellants make a half-hearted attempt to question the October 7 date by pointing out that the examiner did not receive his copy until October 10, but the copy relied on bears a PTO receipt stamp of October 7, amounting to an official record which appellants have not disproved.

***1544** The foregoing facts can be better visualized from the following chart, adapted from one in appellants' brief:

RODGERS et al.	Earliest Proven Date of	
Article	Publication 10/7/74	less than one year

Time			(no time-bar)	
MULDER et al.	7/15/74 Draft Patent	10/9/74 Netherlands	----------	8/6/75 Actual U.S.
Applicants	Application Introduced Into U.S.A. (Conception)	Filing Date Accorded Under 35 U.S.C. § 119	(Constructive Reduction To Practice)	Filing Date

Issues

The primary issue is the obviousness of the invention as defined in the appealed claims in view of the references relied on. Preliminary thereto is the question whether the Rodgers article has been overcome as a reference, and involved in that issue is the question whether appellants are entitled to their Netherlands filing date as a constructive reduction to practice. These questions will be considered in the reverse order of their statement.

OPINION

Adverting to Rule 131, supra, as appellants have shown no actual reduction to practice of the invention in this country and no constructive reduction prior to the date of Rodgers, what Rule 131(b) says they have to show is conception in this country prior to Rodgers' date coupled with "due diligence from said date to * * * the filing of the application." The first question, therefore, is the date of conception in this country. The PTO (both the examiner and the board) have accepted July 15, 1974, the date of receipt in the U.S. of the draft application, as a conception date.

[1] The next question is whether appellants are entitled, as a date of constructive reduction to practice, to the Netherlands or only to the actual U.S. filing date. The examiner said it was the former, the board the latter. We agree with the examiner.

[2] The board cited no authority for depriving appellants of the benefit of their convention filing date; it only remarked that "the events of concern under 37 CFR 1.131 are events that occur in this country." It made no reference to § 119 of the statute. We note that Rule 131 refers to "facts showing a completion of the invention in this country" but we also note that in (b) it makes a distinction between an *actual* reduction to practice (which has to be "in this country") and the "filing of the application." We are also aware of the statute which prohibits reliance on "activity * * * in a foreign country" in establishing "a date of invention," 35 U.S.C. § 104. But that same statute has an express exception--"except as provided in sections 119 and 365 of this title." It is § 119 with which we are concerned. It provides that when a U.S. application has been filed, as was the application in this case, within a year from an application in a convention country such as the Netherlands, the formalities all being complied with, the U.S. application

> * * * shall have the same effect as the same application would have if filed in this country on the date on which the application for patent for the same invention was first filed in such foreign country * * *.

1545** We hold that this provision entitles appellants to rely on their Netherlands filing date for a constructive reduction to practice. Section 119 is a "patent-saving" provision for the benefit of applicants, and an applicant is entitled to rely on it as a constructive reduction to practice to overcome the date of a reference under Rule 131. ***In re Ziegler, 347 F.2d 642, 52 CCPA 1473, 146 USPQ

76 (1965) (convention German filing dates available to overcome references under § 119). If entitlement to a foreign filing date can completely overcome a reference we see no reason why it cannot partially overcome a reference by providing the constructive reduction to practice element of proof required by Rule 131. It is a *statutory* priority right which cannot be interfered with by a construction placed on a PTO rule. *Cf. In re Hilmer,* 359 F.2d 859, 878, 53 CCPA 1288, 1312, 149 USPQ 480, 496 (1966).

This brings us to the next question under Rule 131. Referring to the time chart, supra, appellants have their conception date of July 15, 1974, and their constructive reduction to practice date of October 9, 1974, and Rule 131 requires that these dates must be "coupled with due diligence." Appellants would have us treat this case as though it were an interference between them and Rodgers, treating Rodgers as an applicant for a patent. But Rodgers is not an applicant and this is not an interference. Rodgers is a printed publication which is prior art under 35 U.S.C. § 102(a), unless shown not to be prior, and thus also "prior art" under § 103. Interference rules do not necessarily apply; nothing is to be gained by treating the situation as though it were something it is not. Interferences involve policy questions not present when antedating a reference. The argument is that *if* this were an interference, and *if* Rodgers were an applicant who has not reduced to practice at all, appellants were first to conceive and first to reduce to practice and would not have to prove diligence. This argument "won't fly." This is not an interference. Rule 131 requires proof of diligence coupling conception to the filing of the application.

[3] The next argument is that there is only a two-day period between the Rodgers' effective date and the filing date, that diligence need be shown only from *just prior* to Rodgers' date, that the gap is very short, and that Rule 131 should be "liberally construed." A liberal construction of the rule, which is clearly intended to benefit applicants, will permit applicants to show diligence from just prior to the date of the reference to their convention filing date, rather than all the way from their proven conception date, but liberality cannot be extended to the point of eliminating all proof of diligence, no matter how short the period to be covered. Appellants' difficulty, as they have had to admit, is that there is no evidence whatever of record showing diligence, and therefore they cannot comply with the rule. Focussing on the shortness of the gap is misleading. During the period between the time the draft application was received in this country and the time the application was filed in the U.S. PTO, the record shows no activity of any kind in this country. The only intervening event of record respecting this invention is the filing of the patent application in the Netherlands. Even that was not done until nearly 3 months after the draft U.S. application was dispatched. Under the circumstances, the PTO's refusal to accept the declarations as meeting the requirements of Rule 131 must be affirmed because of a total lack of evidence of diligence to *couple* conception to the filing date--leaving a hiatus--and Rodgers must be treated as prior art.

Appellants assert there is "CCPA authority" contrary to the board's interpretation of Rule 131 which, except for its refusal of the convention filing date for constructive reduction to practice, we approve. We see none. They have relied heavily on *In re Stempel,* 241 F.2d 755, 44 CCPA 820, 113 USPQ 77 (1957). Their reliance is misplaced. While the court there did construe Rule 131 "liberally," and in one respect contrary to its express terms to give Stempel his statutory rights, it was on a point having no bearing on the fact situation here and, more particularly, having nothing to ***1546** do with the necessity for showing diligence. The essence of *Stempel* is that there the facts established by affidavits under Rule 131 did not show that Stempel had completed the generic invention of the rejected claims although they did antedate "all pertinent subject matter" disclosed in the reference. The court held that sufficed, notwithstanding the words "completion of the invention" appearing in the rule. The case had nothing to do with facts such as those controlling here where the issue is not *what* has been antedated but *whether* the reference has been antedated at all.

Another case appellants rely on is *In re Clarke,* 356 F.2d 987, 53 CCPA 954, 199 USPQ 665 (1966). Apparently, that is where they got the expression "possession" of the invention which they use to argue that they were in possession of "everything relevant to the invention disclosed by Rodgers" before the date of that reference. It could be that they were, in the conception sense, but that is not

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the issue. What they must prove in order to have possession is reduction to practice carried back to a date prior to Rodgers by the connecting link of diligence, else they do not have the kind of "possession" *Clarke* and Rule 131 require. The rejection in *Clarke* was affirmed for, among other things, lack of a showing of diligence and we do not see how the case helps appellants, who are not using "possession" in the sense it was used in the *Clarke* opinion.

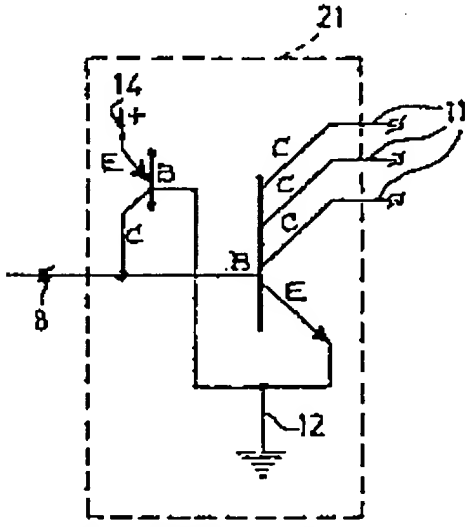
We have examined the other cases cited by appellants and find them of no more help to their contentions than those discussed above.

We turn now to the main issue of obviousness treating Rodgers as prior art.

The Obviousness Issue

a. The claimed invention

The invention of the appealed claims is a particular form of an Integrated Injection Logic (IIL or I 2L) circuit. I 2L circuits contain numerous logic gates each comprising a pair of transistors, one NPN type and one PNP type, one such gate being shown in schematic form within the broken line box 21 in a portion of appellants' Fig. 2:



For each transistor, shown in conventional symbols, the emitter, base, and collector (three collectors in the case of the NPN transistor) have been labeled E, B, and C, respectively. In the arrangement shown, the NPN transistor (on the right) is called the "inverter" transistor, and the PNP transistor (on the upper left) is called the "complementary" transistor. The emitter 14 of the PNP transistor is called the "injector." Note that the collector of the PNP transistor is connected to the base of the NPN transistor, and the base of the PNP transistor is connected to the emitter of the NPN transistor.

A significant feature of this simple arrangement is that the two sets of electrically connected portions of the transistor pair can each share a common physical region of the doped semiconductor material in which they are formed. Thus, the arrangement lends itself to certain clever layouts or "topologies" of variously doped semiconductor material in the design of integrated circuits containing vast arrays of these gates. Appellants disclose an example of their topology in their Fig. 5:

***1547**

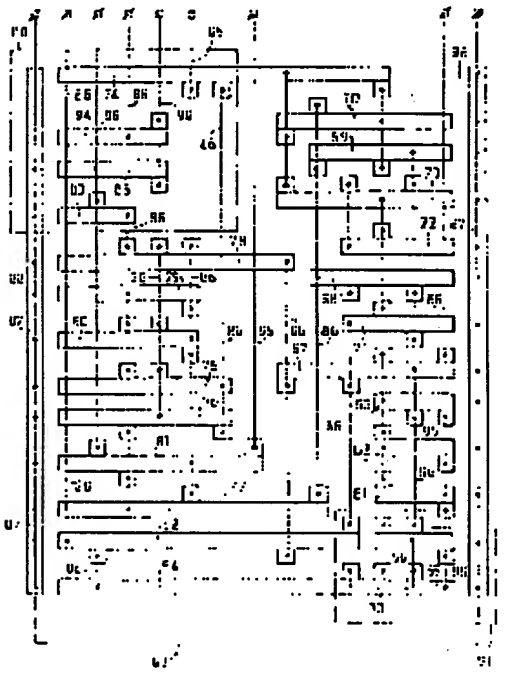


Fig. 5

The PTO solicitor aptly describes this figure in his brief:

> The inverter NPN transistors are layed out in horizontal rows, whereas the conductive metal electrical interconnections are disclosed as

vertical columns 86. Also, the emitters of the complementary PNP transistors are indicated by blocks 87, disclosed as vertical rails or columns on either side of the device, and the conductive metal electrical connections for the PNP transistors are labeled 88. The horizontal blocks 61-85 are the collectors for the PNP transistors, as well as the bases for the NPN transistors. * * * Finally, the unlabeled squares shown adjacent blocks 61-85 are the output collectors for the NPN transistors.

Appellants describe their invention thus:

A principle object of the invention is the provision of an I 2L circuit having a topology or layout which particularly lends itself to the use of computer-aided design, but where the usual loss of packing density previously associated with such techniques is minimized and where there is little sacrifice in the switching speed or delay time of the logic gate circuits.

* * *

The concept embodied in appellants' structure is to provide a column of complementary transistor emitter zones adjacent and parallel to an array of parallel-extending straight conductors or signal tracks. An array of inverter transistor gate circuits occupying different lengths are arranged in rows crossing the signal tracks and extending from a location in the vicinity of the complementary transistor emitter zones. The connections to the base regions and one or more collector regions in each inverter transistor gate circuit are made at the intersections of the straight signal tracks with the base and collector regions, regardless of the lateral spacing between the connections in a given row. That is why the lengths of the rows occupied by some of the gate circuits are different and why the spacing in the base and collector connections in a given row are different from those in another row.

Claim 39 is typical of the claims on appeal:

39. An integrated circuit comprising a common semiconductor body portion, said body portion comprising plural gate circuits each comprising at least one inverter transistor having emitter and base zones and at least one collector, and a complementary transistor connected to the inverter transistor for biasing same and having emitter, base and collector zones with the complementary transistor having its collector zone connected to the inverter transistor base zone, and each gate circuit having means connecting the complementary transistor base zone and the inverter transistor emitter zone in a d.c. path, said inverter transistor being arranged along substantially parallel rows with all the inverter transistor collectors of the same gate circuit being located along the same row and wherein at least some of the gate circuits occupy different lengths in the row direction, ***1548** means for interconnecting inverter transistor collectors and base zones of different gate circuits located in different rows to form desired logic, said inverter transistor collector and base zone interconnecting means comprising a group of elongated signal tracks substantially all of which extend substantially their entire length in mutually parallel straight lines and over the body substantially transversely to the row directions, said signal-track-interconnected collectors in different rows being located under the interconnecting signal track, at least plural tracks in the group of signal tracks interconnecting gate circuits in nonadjacent rows and crossing over at least one gate circuit in an intervening row, a plurality of said gate circuits each having connections to said signal tracks that are spaced apart in the row direction by distances that are different from the spacing of signal track connections to other gate circuits, the biasing complementary transistor emitter zones being located along a column extending parallel to and located alongside the said group of signal tracks, and means for isolating adjacent rows of inverter transistors.

b. The references

The primary reference is Rodgers, which discloses application of a "layout algorithm" to produce an I 2L circuit layout resembling that of appellants except that it has regular rows of doped semiconductor regions all of equal length. Rodgers contains no explanation of why these regions all have the same length.

The article by de Troye discusses some of the trade-offs involved in varying the physical arrangement of the N-type semiconductor with respect to the injector. Also disclosed is an I 2L circuit in which the base regions vary in size and

shape, but in which the circuit components nevertheless form an ordered array.

Agraz-Guerena shows an I 2L circuit having an annular structure which contains heavily doped, low resistivity base regions.

Hart shows an I 2L memory circuit, and a conventional I 2L circuit including the use of electrically insulative material to isolate the separate base regions.

Berger shows the use of separate external PNP current sources in a complementary transistor device which the examiner characterized as a forerunner to I 2L circuitry.

c. The rejections

[4] There are four obviousness rejections, which will be discussed separately. Inasmuch as the solicitor in his brief incorporated by reference the position of the board, it is the board's position which will be set forth in connection with each rejection.

(1) Claims 9, 39-41, and 44 stand rejected as obvious from Rodgers' disclosure of an ordered array of I 2L elements having the same length considered together with de Troye's disclosure of an I 2L device having base regions of varying lengths. The board agreed with the examiner that one skilled in the art would have been motivated to increase the packing density of a Rodgers-type array by making the base regions only as long as necessary as taught by de Troye. Appellants had argued to the board that Rodgers had made all of his bases of equal length in order to achieve the desirable result of equalizing capacitances. However, the board found no basis for this argument in the Rodgers' article, and opined that, even if appellants were correct, equalized capacitance and high packing density were obvious trade-offs. Appellants also argued that the layout of their array lent itself particularly well to computer-aided design. The board rejected this argument as well, because the claims are not limited to computer-aided design, and because it felt that the elements in Rodgers' arrays are also arranged so as to be susceptible to computer-aided design. The board paid special attention to claim 9, which depends from claim 39 and recites additionally "means to reduce the input series resistance of the gate circuits." The board asserted that the arrangement disclosed in de Troye comprised such means.

***1549** On appeal, appellants adhere to their position that to make the gate circuits in Rodgers of varying lengths would be "contrary to the intent of Rodgers." This argument is not convincing. Appellants concede that Rodgers does not reveal why the gates are all the same length, so that there is manifestly no "intent" to which varying length can be contrary. Appellants also repeat their assertions about how their layout lends itself to computer- aided design. They say that de Troye's layout is not a matrix-ordered array, and so, presumably, not as well suited to computer-aided design. Rodgers, however, is manifestly a matrix-ordered layout, and appellants have not shown what differences between their invention and what is suggested by Rodgers and de Troye considered together would make their invention superior for computer- aided design.

With respect to claim 9, we note that it is drafted in "means plus function" format, so that it is "construed to cover the corresponding structure * * * described in the specification and equivalents thereof." 35 U.S.C. § 112. As stated above, the board said that de Troye's arrangement constituted means to reduce input series resistance. Appellants have neither asserted nor shown that de Troye's structure is not the equivalent of the structure disclosed in their specification for reducing input series resistance.

In view of the above, we affirm the decision of the board with respect to the above rejection of claims 9, 39-41, and 44.

(2) Claims 9 and 42 stand rejected for obviousness from Rodgers and de Troye as discussed, together with Agraz-Guerena's disclosure of heavily doped, low resistivity base portions. Appellants argued to the board that it would not have been obvious to use the teachings of Agraz-Guerena in a matrix I 2L array because Agraz-Guerena teaches an annular structure. The board saw no reason why such a structure would not be suitable in a matrix array, and in addition noted that claims 9 and 42 are not limited to appellants' disclosed comb-type array. On appeal, appellants repeat their conclusory

assertion that Agraz- Guerena's annular structure would have made application of its teachings to a comb-type structure nonobvious. In the absence of specifics or evidence as to why this is the case, we cannot say that the board erred in affirming the examiner's rejection. Hence, the board's decision with respect to this rejection is affirmed.

(3) Claims 2-4 stand rejected on Rodgers and de Troye together with Hart's disclosure showing the physical structure of a conventional I 2L circuit. Both before the board and this court appellants have not argued that claims 2-4 recite patentable subject matter independently of claim 39, from which they depend. Inasmuch as we have affirmed the board's decision with respect to claim 39, we affirm it with respect to claims 2-4 as well.

(4) Finally, claims 31-33 stand rejected on Rodgers, considered together with Hart's teaching of a conventional I 2L circuit structure, and Berger's teaching of separate current sources. The board said that in view of these combined teachings, the use of an external conductor to couple the inverter base and current source collector would have been obvious. The board also stated that Hart suggests internally coupling transistor regions, and noted that claims 31- 33 do not appear to distinguish over what appellants had illustrated as prior art in Fig. 1 of their application.

The board's affirmance of this rejection is the only decision on nonobviousness which appellants addressed in their request to the board for reconsideration. Therein they said that Berger does not show the electrical connection between the complementary transistor base zone and the inverter transistor emitter zone and at the same time an external connection between the complementary transistor collector zone and to the inverter transistor base zone as specified in claim 31. Appellants also contest the board's assertion that claims 31-33 read on what appellants labeled prior art in their specification. In denying the request for reconsideration, the board emphasized that the rejection had been premised on Berger *together with* Rodgers and Hart, not on ***1550** Berger alone, and that Berger did indeed show those features for which it had been cited. The board also reaffirmed its belief that claims 31-33 read on conceded prior art.

On appeal, appellants now assert that Berger has "no relevance to appellants' gate array" and that the teachings of Rodgers and Hart cannot be combined with those of Berger to "render the present invention obvious." Appellants then proceed to assail the board's decision with exactly the same arguments which were unavailing before the board.

We find these arguments unpersuasive. Appellants offer only unsupported conclusions which find no basis in any evidence of record. In short, we find appellants' mere repetition of arguments fully answered by the board. To obtain reversal, appellants must clearly explain why the board decision on those arguments is wrong, not merely repeat arguments made to the board hoping for a different result. We therefore affirm the decision of the board with respect to claims 31-33.

The decision of the board affirming rejections of all appealed claims, 2-4, 9, 31-33, 39-42, and 44 is *affirmed.*

AFFIRMED.

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